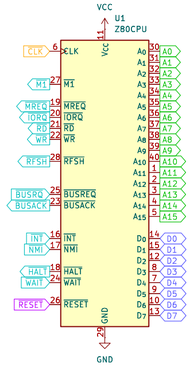
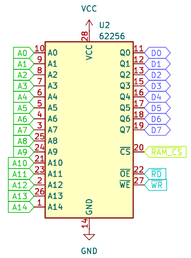
Z80 CPU



System RAM

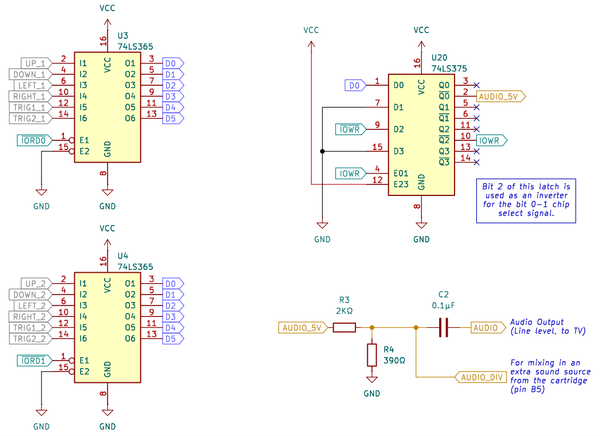
(16KB used as system RAM, 8KB used as video RAM mirror)



The CPU is unable to read from video RAM directly, but all data that is written to video RAM is simultaneously written to system RAM.

Therefore, it's possible to read the contents of video RAM from system RAM.

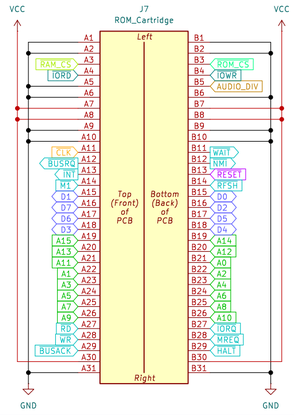
Controller Inputs, Audio Output



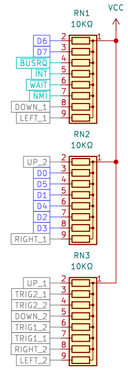
Bit 2 of this latch is used as an inverter for the bit 0–1 chip select signal.

ROM Cartridge Slot

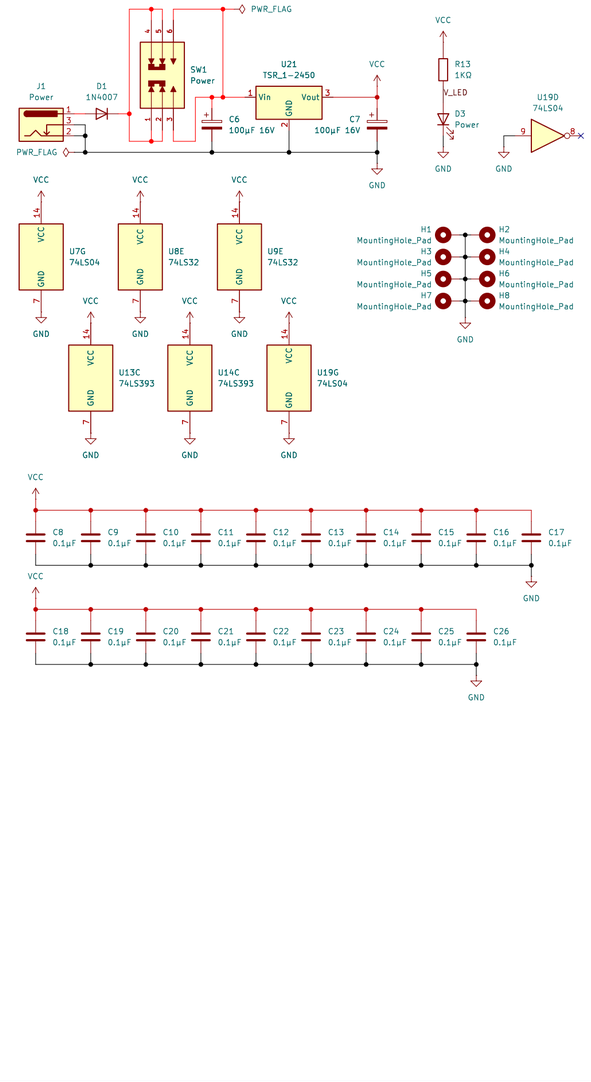
62-pin edge connector, 2.54mm pin spacing (identical to 8-bit ISA connectors)



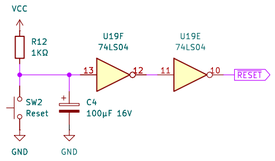
Pullup Resistors



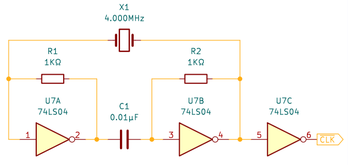
Power Circuitry



Reset



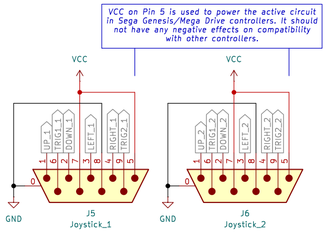
4MHz Clock Generator



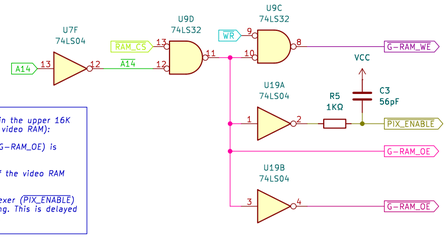
Controller Connectors

VCC on Pin 5 is used to power the active circuit in Sega Genesis/Mega Drive controllers. It should not have any negative effects on compatibility with other controllers.

Compatible controllers:	TRIG1	TRIG2
Atari 2600/Generic 1-Button	Fire	N/A
Sega Master System	1	2
Sega Genesis/Mega Drive	B	C



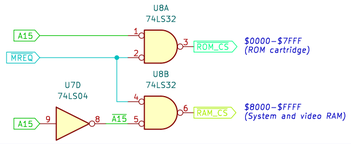
Video Control



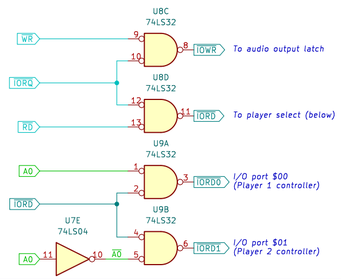
When memory is accessed in the upper 16K address space (location of video RAM):

- Video RAM data output (G-RAM_OE) is disabled.
- The CPU takes control of the video RAM address bus.
- The video output multiplexer (PIX_ENABLE) is disabled while writing. This is delayed slightly by R5 and C3.

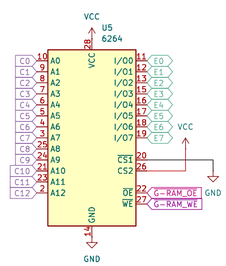
Memory Select



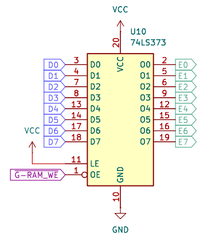
I/O Select



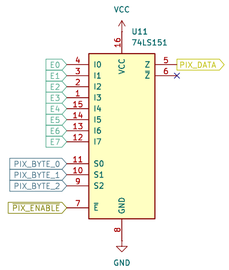
Video RAM (8KB)



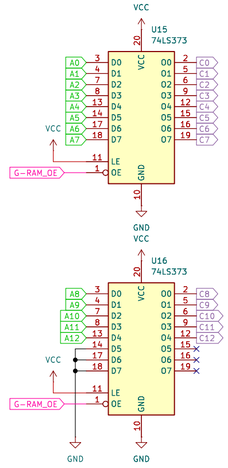
System to VRAM Data Buffer



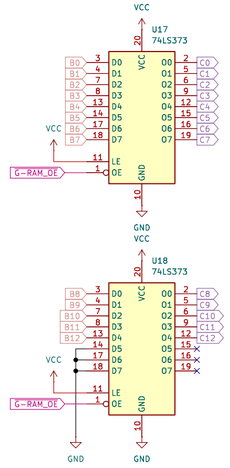
VRAM to Video Output Multiplexer



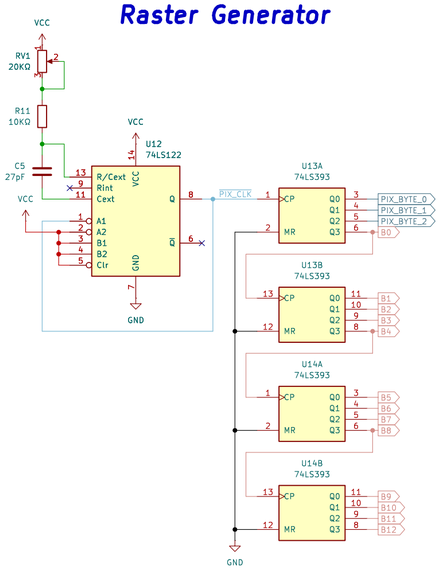
System to VRAM Address Buffer



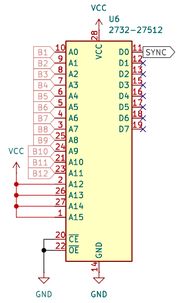
VRAM to Video Output Address Buffer



Raster Generator



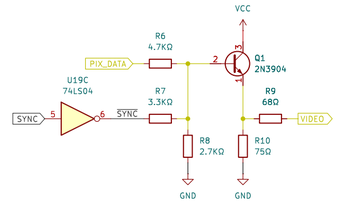
Sync Generator



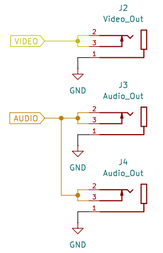
This IC can be any (E)EPROM with a capacity between 4KB (2732) to 64KB (27512)... which is good, since the access time requirements are fairly stringent.

I have had good results with an Atmel AT28C64-15PC (150ns access time)

Video Output



A/V Connectors



Z80のテレビゲーム2
Original circuit designed by Mr. Isizu – http://w01.tp1.jp/~a571632211
A=System address, D=System data, C=VRAM address, E=VRAM data, B=Sync gen. address

Alex J. Lowry (alex-j-lowry.github.io)

Sheet: /
File: Z80_TV_Game.kicad_sch

Title: Z80 TV Game 2

Size: A2	Date: 2026-03-07	**Rev: 1**
KiCad E.D.A. 9.0.7		Id: 1/1