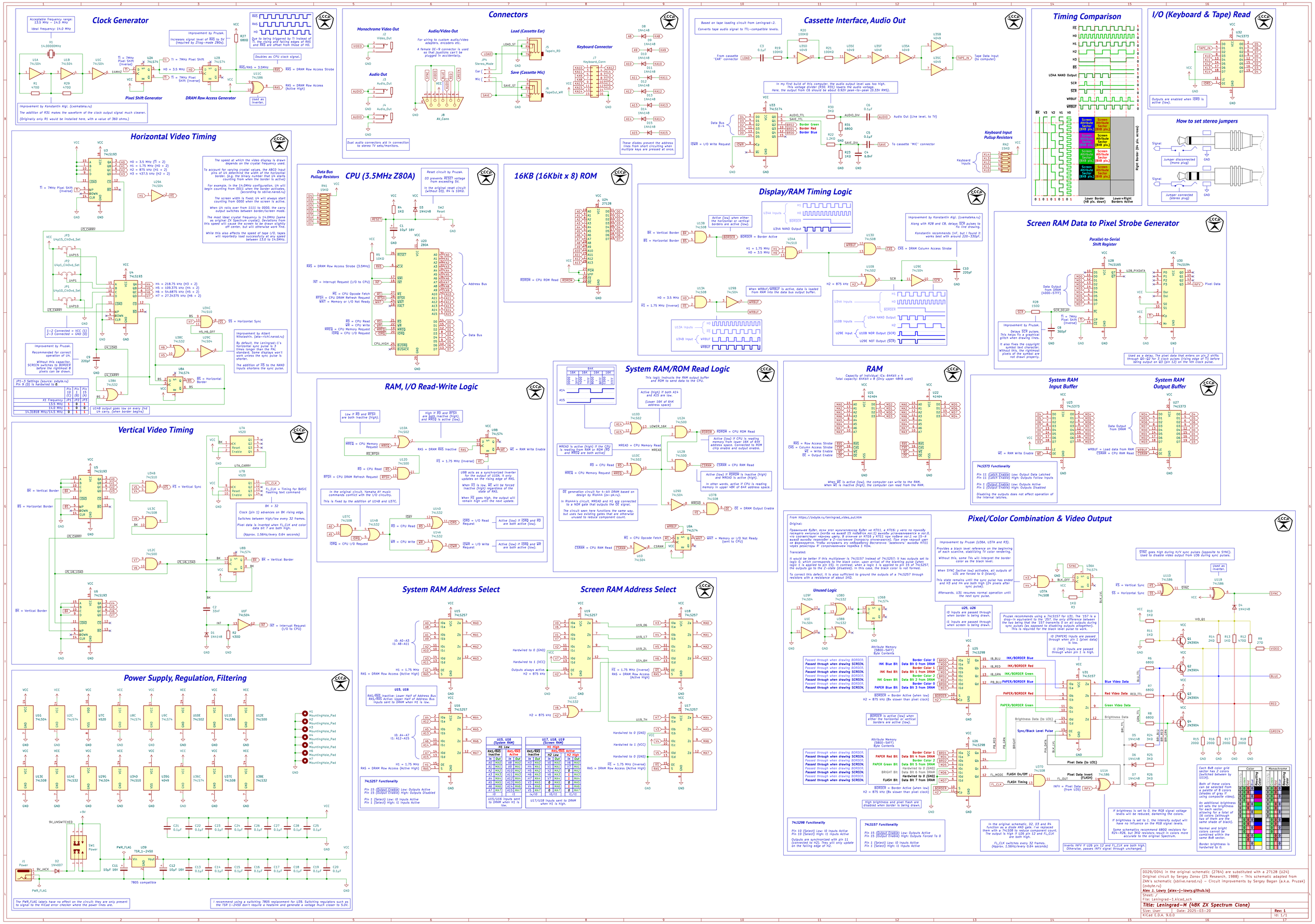
Clock Generator
Acceptable frequency range: 13.5 MHz – 14.5 MHz
Ideal frequency: 14.0 MHz
X1 14.00000MHz
U1A 74LS04
U1B 74LS04
U1C 74LS04
R1 470Ω
R29 470Ω
14MHz
Pixel Shift Generator
Improvement by Pruzak.
Increases signal level of RAS to 5V (required by Zilog-made Z80s).
R27 680Ω
Due to being triggered by TI instead of TI, the rising and falling edges of RAS and RAS are offset from those of HO.
U2A 74LS74
U2B 74LS74
TI = 7MHz Pixel Shift (Inverse)
HO = 3.5 MHz
RAS/RAS = 3.5MHz
RAS = DRAM Row Access Strobe
U11C 74LS86
Used as inverter.
DRAM Row Access Generator
Doubles as CPU clock signal.
RAS = DRAM Row Access (Active High)
Improvement by Konstantin Algl. (cvemateka.ru)
The addition of R31 makes the waveform of the clock output signal much cleaner.
(Originally only R1 would be installed here, with a value of 360 ohms.)
Connectors
Monochrome Video Out
J2 Video_Out
VIDEO
GND
Audio Out
J3 Audio_Out
J4 Audio_Out
AUDIO
Dual audio connectors aid in connection to stereo TV sets/monitors.
Audio/Video Out
For wiring to custom audio/video adapters, encoders etc.
A female DE-9 connector is used so that joysticks can't be plugged in accidentally.
SYNC
VIDEO
BLUE
RED
GREEN
VCC
GND
J8 AV_Conn
Load (Cassette Ear)
LOAD_ST
LOAD
Stereo_Mode
Ear
J5 Tape_In_RD
Save (Cassette Mic)
SAVE_ST
SAVE
Mic
J6 Tape_Out_WR
Keyboard Connector
J7 Keyboard_Conn
KA10
KA11
KA12
KA13
KA14
KA15
KL0
KL1
KL2
KL3
KL4
KL5
D8 1N4148
D9 1N4148
D10 1N4148
D11 1N4148
D12 1N4148
D13 1N4148
D14 1N4148
D15 1N4148
These diodes prevent the address lines from short circuiting when multiple keys are pressed at once.
Cassette Interface, Audio Out
Based on tape loading circuit from Leningrad-2.
Converts tape audio signal to TTL-compatible levels.
From cassette "EAR" connector
C3 0.1μF
R19 100KΩ
R20 100KΩ
R21 100KΩ
U35B 4049
U35C 4049
TAPE_IN
Tape Data Input (to computer)
In my first build of this computer, the audio output level was too high.
This voltage divider (R30, R31) lowers the audio voltage.
Here, the output from C6 should be about 0.92V peak-to-peak (0.33V RMS).
U33 74LS174
Data Bus 0–5
IOWR = I/O Write Request
AUDIO_TTL
SAVE_TTL
BORD2 Border Green
BORD1 Border Red
BORD0 Border Blue
R30 3KΩ
R31 680Ω
R22 1.2KΩ
R23 1KΩ
C6 0.1μF
C5 0.1μF
C4 6.8nF
AUDIO_DIV
SAVE_DIV
AUDIO
SAVE
Audio Out (Line level, to TV)
To cassette "MIC" connector
Keyboard Input Pullup Resistors
RN2 15KΩ
Keyboard Inputs
Timing Comparison
HI
H0
H1
H2
H3
BS
U34A NAND Output
SCR
SCR
WRBUF
WRBUF
BK
V3
V2
V1
V0
Screen Attribute Sector (8x8 pix.)
Right Border (64 pix. across)
Lower Border (48 pix. down)
Lower+Right Borders Active
I/O (Keyboard & Tape) Read
U32 74LS373
TAPE_IN
KL0
KL1
KL2
KL3
KL4
IORD
Outputs are enabled when IORD is active (low).
How to set stereo jumpers
Signal
Jumper disconnected (mono plug)
Jumper connected (stereo plug)
Horizontal Video Timing
U3 74LS193
H0 = 3.5 MHz (TI ÷ 2)
H1 = 1.75 MHz (H0 ÷ 2)
H2 = 875 kHz (H1 ÷ 2)
H3 = 437.5 kHz (H2 ÷ 2)
U29A 74LS04
U3_CARRY
JP3 U4p15_Clk0=I_Set
JP2 U4p1_Clk0=I_Set
JP1 U4p10_Clk0=I_Set
U4p15
U4p1
U4p10
U4 74LS193
H4 = 218.75 kHz (H3 ÷ 2)
H5 = 109.375 kHz (H4 ÷ 2)
H6 = 54.6875 kHz (H5 ÷ 2)
H7 = 27.34375 kHz (H6 ÷ 2)
U4_CARRY
U4_LOAD
J1–2 Connected = VCC (1)
2–3 Connected = GND (0)
The speed at which the video display is drawn depends on the crystal frequency used.
To account for varying crystal values, the ABCD input pins of U4 determine the width of the horizontal border. (e.g. the binary number that U4 starts counting from when the border is active)
For example, in the 14.0MHz configuration, U4 will begin counting from 0011 when the border activates. (according to sblive.narod.ru)
The screen width is fixed: U4 will always start counting from 0000 when the screen is active.
When U4 rolls over from 1111 to 0000, the carry output switches between border/screen mode.
The most ideal crystal frequency is 14.0MHz (same as original ZX Spectrum crystal). Deviations from this speed will cause the screen to be drawn slightly off center, but will otherwise work fine.
While this also affects the speed of tape I/O, tapes will reportedly load successfully at any speed between 13.0 to 14.5MHz.
Improvement by Pruzak.
Recommended for correct operation of U4.
Without this capacitor, SCREEN switches to BORDER before the rightmost 8 pixels can be drawn.
C9 220pF
U34C 74LS10
BS
VS = Horizontal Sync
HS_H6_OFF
U29C 74LS10
U38C 74LS32
H6
U8A 74LS74
BS_2
U38A 74LS32
BS = Horizontal Border
Improvement by Albert Nikolashin. (aka-richi.narod.ru)
By default, the Leningrad-1's horizontal sync pulse is 3 times longer than the PAL standard. Some displays won't work unless the sync pulse is shorter.
The addition of VS to the NAND inputs shortens the sync pulse.
JP1–3 Settings (source: sblive.ru)
Pin 9 (0) is hardwired to GND.
X1 Frequency | JP1 (C) | JP2 (B) | JP3 (A)
13.5 MHz | 1 | 0 | 1
14.0 MHz | 1 | 0 | 0
14.31818 MHz/14.5 MHz | 0 | 1 | 1
U34B output goes low on every 2nd U4 carry. (when border begins)
Data Bus Pullup Resistors
RN1 15KΩ
CPU (3.5MHz Z80A)
Reset circuit by Pruzak.
D3 prevents RESET voltage from exceeding 5V.
In the original reset circuit (without D3), R4 is 10KΩ.
R4 1KΩ
D3 1N4148
SW2 Reset
RESET
C1 10μF 16V
R5 10KΩ
U20 Z80A
RAS = DRAM Row Access Strobe (3.5MHz)
INT = Interrupt Request (I/O to CPU)
WE = CPU Opcode Fetch
RFSH = CPU DRAM Refresh Request
WAIT = Memory or I/O Not Ready
RD = CPU Read
WR = CPU Write
MREQ = CPU Memory Request
IORQ = CPU I/O Request
Address Bus
Data Bus
16KB (16Kbit x 8) ROM
U24 27128
ROMCS = CPU ROM Read
Display/RAM Timing Logic
Active (low) when either the horizontal or vertical borders are active (low).
BK = Vertical Border
BS = Horizontal Border
BORDER = Border Active
U34A 74LS10
U34A NAND Output
U13B 74LS08
H1 = 1.75 MHz
H0 = 3.5 MHz
U13A 74LS08
U29B 74LS04
H1 = 1.75 MHz (Inverse)
U13A Inputs
U34B Input
WRBUF
When WRBUF/WRBUF is active, data is loaded from RAM into the data bus output buffer.
Improvement by Konstantin Algl. (cvemateka.ru)
Along with R28 and C8, delays SCR pulses to fix line drawing.
Konstantin recommends 1nF, but I found it works best with around 220–330pF.
U13D 74LS08
CAS
CAS = DRAM Column Access Strobe
U10B 74LS02
H2 = 875 kHz
SCR
U29E 74LS04
C10 220pF
U34A Inputs
U10B Inputs
U29E Input
U10B NOR Output (SCR)
U29E NOT Output (SCR)
Screen RAM Data to Pixel Strobe Generator
Parallel-to-Serial Shift Register
U28 74LS165
U28_PIXDATA
U30 74LS194
Data Output from DRAM (4000–57FF)
SCR_DELAY
R28 150Ω
C8 360pF
Improvement by Pruzak.
Delays SCR pulses. This helps fix a graphical glitch when drawing lines.
It also fixes the copyright symbol in the BASIC ROM. Without this, the rightmost pixels of the symbol are not drawn properly.
Pixel Data
Used as a delay. The pixel data that enters on pin 2 shifts through Q0–Q2 for 3 clock pulses (rising edge of TI) before being output on Q3 (pin 12) on the 4th clock pulse.
Vertical Video Timing
U7A 4520
U7B 4520
Reset
Enable
U7A_CARRY
FL_CLK
FL_CLK = Timing for BASIC flashing text command
U5 74LS193
U5_CARRY
U5_U6_LOAD
U6 74LS193
U34B 74LS10
VS = Vertical Sync
U13C 74LS08
U12C 74LS00
U8B 74LS74
BK = Vertical Border
BK = 32
Clock (pin 1) advances on BK rising edge.
Switches between high/low every 32 frames.
Pixel data is inverted when FL_CLK and color data bit 7 are both high.
(Approx. 1.56Hz/every 0.64 seconds)
C2 33nF
U1F 74LS04
INT = Interrupt Request (I/O to CPU)
D4 1N4148
R2 430Ω
RAM, I/O Read-Write Logic
Low if RD and RFSH are both inactive (high).
High if RD and RFSH are both inactive (high) and MREQ is active (low).
U10A 74LS02
U9B 74LS74
MREQ = CPU Memory Request
RD_RFSH
RAS = DRAM RAS Inactive
WE = RAM Write Enable
U20 74LS00
RD = CPU Read
RFSH = CPU DRAM Refresh Request
U9B acts as a synchronized inverter for the output of U10A. It only updates on the rising edge of RAS.
When WE is low, WE will be forced inactive (high) regardless of the state of RAS.
When WE goes high, the output will remain high until the next update.
In the original circuit, Yamaha AY music commands conflict with the I/O circuitry.
This is fixed by the addition of U14B and U37C.
U37C 74LS08
U14B 74LS32
IORQ = CPU I/O Request
U14D 74LS32
U14A 74LS32
WR = CPU Write
IORD = I/O Read Request
Active (low) if IORD and RD are both active (low).
IOWR = I/O Write Request
Active (low) if IORD and WR are both active (low).
System RAM/ROM Read Logic
This logic instructs the RAM output buffer and ROM to send data to the CPU.
64K
16K
A14
A15
Active (high) if both A14 and A15 are low.
(lower 16K of 64K address space)
U10D 74LS02
U12A 74LS00
LOWER_16K
ROMCS = CPU ROM Read
MREAD is active (high) if the CPU is reading from RAM or ROM (RD and MREQ are both active)
MREAD = CPU Memory Read
Active (low) if CPU is reading memory in lower 16K of 64K address space. Connected to ROM chip enable and output enable.
U12B 74LS00
CSRAM = CPU RAM Read
Active (low) if ROMCS is inactive (high) and MREAD is active (high).
In other words, when CPU is reading memory in upper 48K of 64K address space.
U29D 74LS04
U37B 74LS08
OE = DRAM Output Enable
OE generation circuit for 4-bit DRAM based on design by Rip444 (zx-pk.ru).
In Rip444's circuit, MREAD and RD are connected to a NOR gate that outputs the OE signal.
The circuit seen here functions the same way, but uses two existing gates that are otherwise unused to reduce component count.
U9A 74LS74
WAIT = Memory or I/O Not Ready (sent to CPU)
U10 74LS04
RAM
Capacity of individual ICs: 64Kbit x 4
Total capacity: 64KB x 8 (Only upper 48KB used)
U21 41464
U22 41464
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MD0
MD1
MD2
MD3
RAS = Row Access Strobe
CAS = Column Access Strobe
WE = Write Enable
OE = Output Enable
When WE is active (low), the computer can write to the RAM. When WE is inactive (high), the computer can read from the RAM.
System RAM Input Buffer
U23 74LS373
WE = RAM Write Enable
System RAM Output Buffer
U27 74LS373
Data Output from DRAM
WRBUF = Load data from RAM
CSRAM = CPU RAM Read
74LS373 Functionality
Pin 11 (Latch Enable) Low: Output Data Latched
Pin 11 (Latch Enable) High: Outputs Follow Inputs
Pin 1 (Output Enable) Low: Outputs Active
Pin 1 (Output Enable) High: Outputs Disabled
Disabling the outputs does not affect operation of the internal latches.
Pixel/Color Combination & Video Output
From https://zxbyte.ru/leningrad_video_out.htm
Original:
Правильнее будет, если этот мультиплексор будет на К174, а К1table у него по прежнему гасящего импульса (когда на выводе 15 подается ноль) выводы устанавливаются в ноль, что соответствует черному цвету. В отличие от К1table у К174 при подаче ноль на 15-й вывод выходы переходят в Z-состояние (попросту отключаются). При этом черный цвет не формируется. Чтобы исправить это недоразбору достаточно "заземлить" выводы К174 через резистор R сопротивлением порядка 1 КОм.
Translated:
It would be better if this multiplexer is 74LS157 instead of 74LS257: it has outputs set to logic 0, which corresponds to the black color, upon arrival of the blanking pulse (when logic 1 is applied to pin 15). In contrast, when a logic 1 is applied to pin 15 of 74LS257, the outputs go to the Z-state (disabled). In this case, the black color is not formed.
To correct this defect, it is also sufficient to ground the outputs of a 74LS257 through resistors with a resistance of about 1KΩ.
Unused Logic
U29F 74LS04
U1E 74LS04
U38D 74LS32
U38B 74LS32
U38C 74LS32
U36B 74LS74
Attribute Memory (5800–5AFF) Byte Contents
Passed through when drawing BORDER.
Passed through when drawing SCREEN.
INK Blue Bit
INK Red Bit
INK Green Bit
PAPER Blue Bit
Border Color 0
Data Bit 0 from DRAM
Border Color 1
Data Bit 1 from DRAM
Border Color 2
Data Bit 2 from DRAM
Border Color 0
Data Bit 3 from DRAM
BORDER = Border Active (when low)
H2 = 875 kHz (8x slower than pixel clock)
BORDER is active (low) when either the horizontal or vertical borders are active (low).
U25 74LS298
INK/BORDER Blue
INK/BORDER Red
INK/BORDER Green
PAPER/BORDER Blue
PAPER/BORDER Red
PAPER/BORDER Green
Sync/Black Level Pulse
Pixel Data (to U31)
PAPER Red Bit
PAPER Green Bit
BRIGHT Bit
Hardwired to 0 (GND)
Data Bit 7 from DRAM
U26 74LS298
Brightness Data (to U31)
FLASH On/Off
FLASH Timing
FL_MODE
FL_CLK
FL_OUT
U37D 74LS08
Pixel Data Invert (FLASH)
INFV = Pixel Data (from U35)
U11A 74LS86
High brightness and pixel flash are disabled when border is being drawn.
Improvement by Pruzak (U36A, U37A and R3).
Provides a black level reference on the beginning of each scanline, stabilizing TV color rendering.
Without this, some TVs will interpret the border color as the black level.
When SYNC (active low) activates, all outputs of U31 are forced to 0 (black).
This state remains until the sync pulse has ended and H0 and H4 are both high (24 pixels after sync pulse).
Afterwards, U31 resumes normal operation until the next sync pulse.
U36A 74LS74
U37A 74LS08
BLK_LVL
U25, U26
I0 inputs are passed through when border is being drawn.
I1 inputs are passed through when screen is being drawn.
Pruzak recommends using a 74LS157 for U31. The '157 is a pin-compatible equivalent to the '257, the only difference between the two being that the '157 transmits 0 on all outputs during sync pulses (as opposed to disabling outputs altogether). This is required for the black level pulse to work.
I0 (PAPER) inputs are passed through when pin 1 (pixel data) is low.
I1 (INK) inputs are passed through when pin 1 is high.
U31 74LS157
Blue Video Data
Red Video Data
Green Video Data
Brightness Data
PIX_DATA
BLK_LVL
BRIGHT
PIX_RTD
PIX_GRN
BRI_TTL
BLU_TTL
RED_TTL
GRN_TTL
BRI_RTD
BLU_RTD
RED_RTD
GRN_RTD
D5 1N4148
D6 1N4148
D7 1N4148
R24 3KΩ
R25 3KΩ
R26 3KΩ
In the original schematic, D2, D3 and R4 function as a diode AND gate. I've replaced them with a 74LS08 to reduce component count. The output is high if U26 pin 12 and FL_CLK are both high.
FL_CLK switches every 32 frames. (Approx. 1.56Hz/every 0.64 seconds)
Inverts INFV if U26 pin 12 and FL_CLK are both high. Otherwise, passes INFV signal through unchanged.
If brightness is set to 0, the RGB signal voltage levels will be reduced, darkening the colors.
If brightness is set to 1, the intensity output will have no influence on the RGB signal levels.
Some schematics recommend 680Ω resistors for R24–R26, but 3KΩ resistors result in colors more accurate to the original Spectrum.
SYNC goes high during H/V sync pulses (opposite to SYNC). Used to disable video output from U36 during sync pulses.
Used as inverter.
U11D 74LS86
U11B 74LS86
VS = Vertical Sync
HS = Horizontal Sync
SYNC
D4 1N4148
R10 1KΩ
VID_Q1
R11 1KΩ
R14 2KΩ
R13 1KΩ
R12 470Ω
R9 270
Q1 2N3904
Q2 2N3904
Q3 2N3904
Q4 2N3904
VIDEO
BLUE
RED
GREEN
R6 680Ω
R7 680Ω
R8 680Ω
R15 200Ω
R16 200Ω
R17 200Ω
R18 200Ω
Each 8x8 color grid sector has 2 colors (switched between by U11A).
Both of these colors can be selected from a palette of 8 colors (shades of gray if using composite video).
An additional brightness bit sets the brightness for each sector, allowing for a total of 16 colors (though two of them are the same shade of black).
Normal and bright colors cannot be combined within the same 8x8 sector.
Border brightness is hardwired to 0.
Color
Bright
Flash
Paper Red
Paper Green
Paper Blue
Ink Red
Ink Green
Ink Blue
Monochrome
Bright
Flash
Paper
Ink
Power Supply, Regulation, Filtering
U1G 74LS04
U2C 74LS74
U7C 4520
U8C 74LS74
U9C 74LS74
U10E 74LS02
U11E 74LS86
U12E 74LS00
U13E 74LS08
U14E 74LS32
U29G 74LS04
U34D 74LS10
U35G 4049
U36C 74LS74
U37E 74LS08
U38E 74LS32
H1
H2
H3
H4
H5
H6
H7
MountingHole_Pad
+9V
9V_UNSWITCHED
SW1 Power
J1 Power
9V_JACK
D2 1N4007
PWR_FLAG
U39 TSR_1-2450
7805 compatible
C11 10μF 16V
C12 10μF 16V
C21 0.1μF
C22 0.1μF
C23 0.1μF
C24 0.1μF
C25 0.1μF
C26 0.1μF
C27 0.1μF
C28 0.1μF
C13 0.1μF
C14 0.1μF
C15 0.1μF
C16 0.1μF
C17 0.1μF
C18 0.1μF
C19 0.1μF
C20 0.1μF
The PWR_FLAG labels have no effect on the circuit; they are only present to signal to the KiCad error checker where the power lines are.
I recommend using a switching 7805 replacement for U39. Switching regulators such as the TSR 1-2450 don't require a heatsink and generate a voltage much closer to 5.0V.
System RAM Address Select
U15 74LS257
U16 74LS257
A0–A3
A4–A7
A8–A11
A12–A15
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
I0: A0–A3
I1: A8–A11
I0: A4–A7
I1: A12–A15
H1 = 1.75 MHz
RAS = DRAM Row Access (Active High)
U15, U16
RAS/RAS Inactive: Lower Half of Address Bus
RAS/RAS Active: Upper Half of Address Bus
Inputs sent to DRAM when H1 is low.
74LS257 Functionality
Pin 15 (Output Enable) Low: Outputs Active
Pin 15 (Output Enable) High: Outputs Disabled
Pin 1 (Select) Low: I0 Inputs Active
Pin 1 (Select) High: I1 Inputs Active
U15, U16 (System RAM)
RAS/RAS Inactive: In | Out | RAS/RAS Active: In | Out
A0 | MA0 | A8 | MA0
A1 | MA1 | A9 | MA1
A2 | MA2 | A10 | MA2
A3 | MA3 | A11 | MA3
A4 | MA4 | A12 | MA4
A5 | MA5 | A13 | MA5
A6 | MA6 | A14 | MA6
A7 | MA7 | A15 | MA7
I0 | I1
U15/U16 Inputs sent to DRAM when H1 is low.
Screen RAM Address Select
U19 74LS257
U17 74LS257
U18 74LS257
Hardwired to 0 (GND)
Hardwired to 1 (VCC)
Outputs always active. H2 = 875 kHz
U14C 74LS32
H2 = 875 kHz
U19_06
U19_17
U19_2L
U14_6H
U19_7H
H1 = 1.75 MHz (Inverse)
U17, U18, U19 (Screen RAM)
H1 Low: RAS/RAS Inactive: In | Out | RAS/RAS Active: In | Out
H2 Low: In | Out | H2 High: In | Out
H3 | MA0 | H3 | MA0
H4 | MA1 | H4 | MA1
H5 | MA2 | V2 | MA2 | 0 | MA2
H6 | MA3 | V6 | MA3 | 1 | MA3
H7 | MA4 | V7 | MA4 | 1 | MA4
V3 | MA5 | 0 | MA5 | 0 | MA5
V4 | MA6 | 1 | MA6 | 1 | MA6
V5 | MA7 | 0 | MA7 | 0 | MA7
In/50 | In/51 | 11/1E
U17/U18 Inputs sent to DRAM when H1 is high.
D029/D041 in the original schematic (2764) are substituted with a 27128 (U24)
Original circuit by Sergey Zonov (ZS Research, 1988) — This schematic adapted from ZAN's schematic (sblive.narod.ru) — Circuit improvements by Sergey Bagan (a.k.a. Pruzak) (zxbyte.ru)
Alex J. Lowy (alex-j-lowy.github.io)
Sheet: /
File: Leningrad-1.kicad_sch
Title: Leningrad-M (48K ZX Spectrum Clone)
Size: User
Date: 2025-03-20
Rev: 1
KiCad E.D.A. 9.0.0
Id: 1/1