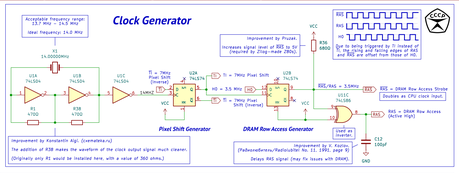
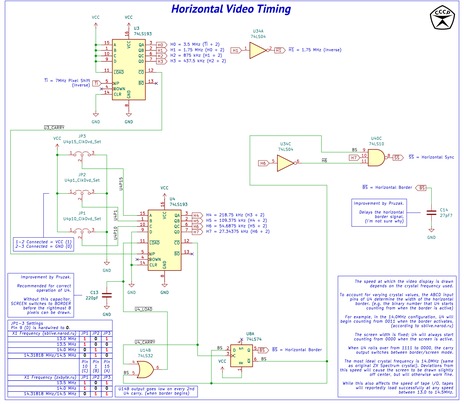
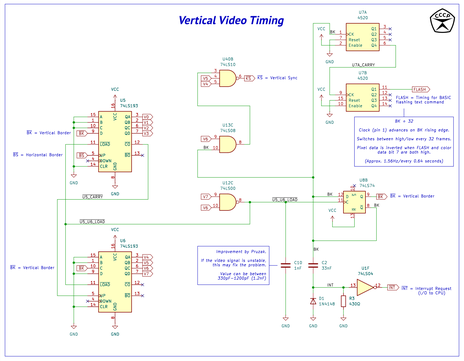
Clock Generator



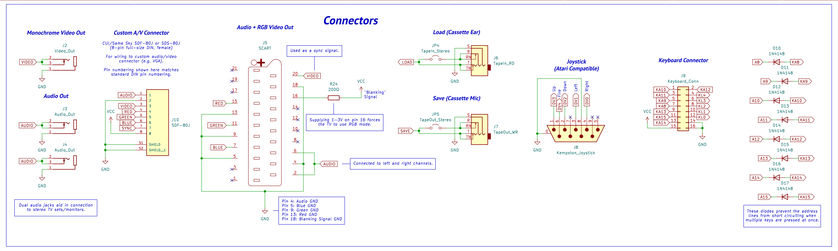
Horizontal Video Timing



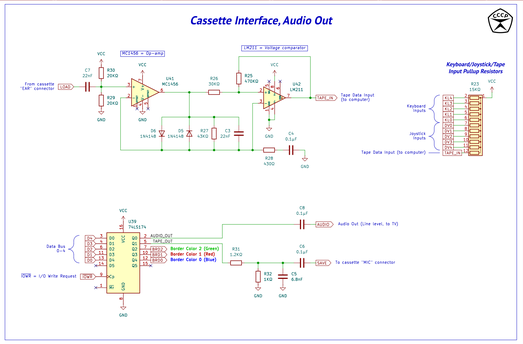
Vertical Video Timing



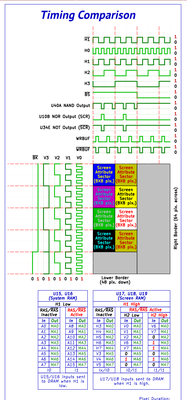
Connectors



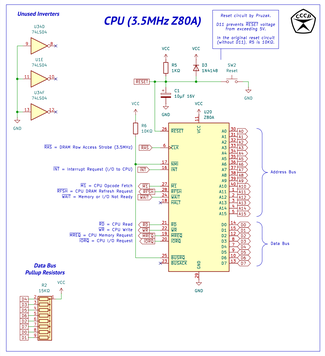
Cassette Interface, Audio Out



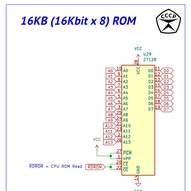
Timing Comparison



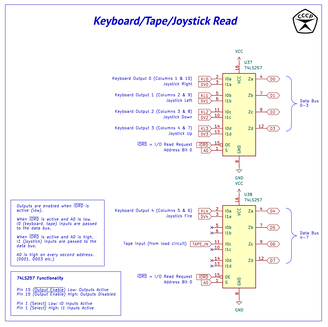
CPU (3.5MHz Z80A)



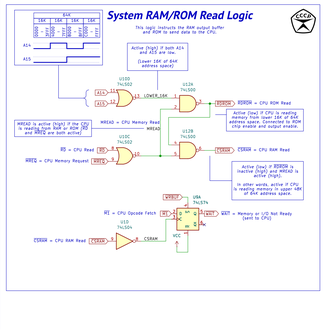
16KB (16Kbit x 8) ROM



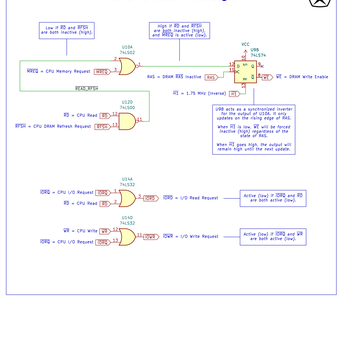
Keyboard/Tape/Joystick Read



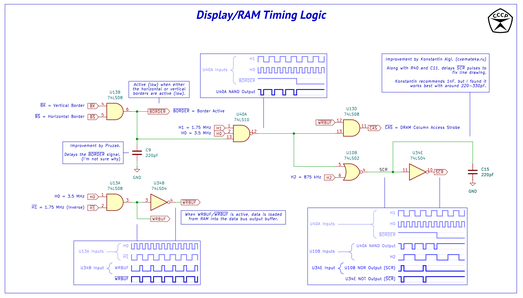
System RAM/ROM Read Logic



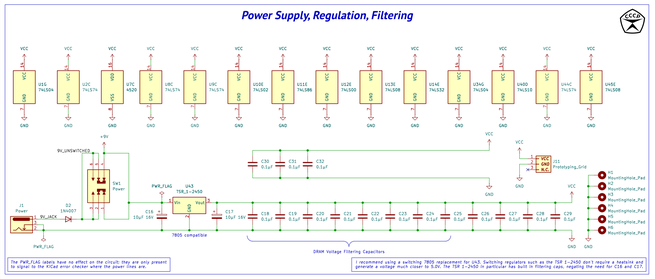
RAM, I/O Read-Write Logic



Display/RAM Timing Logic



Power Supply, Regulation, Filtering



U1 – Basic frequency generator
U4 – Frequency generators for VIDEO CONTROLLER (address selecting & screen generating) and other internal devices (1)
U5 – Frequency generators for VIDEO CONTROLLER (address selecting & screen generating) and other internal devices (2)
U6 – Frequency generators for VIDEO CONTROLLER (address selecting & screen generating) and other internal devices (3)
U7 – FLASH generator
U11D – Combination of vertical and horizontal synchronization pulses
U13B – (BORDER) BORDER/SCREEN drawing
U13C – Vertical synchronization pulses (1)
U15 – CPU address multiplexers (1)
U16 – CPU address multiplexers (2)
U17 – VIDEO CONTROLLER address multiplexers (1)
U18 – VIDEO CONTROLLER address multiplexers (2)
U19 – VIDEO CONTROLLER address multiplexers (3)
U30 – Switcher of BORDER/SCREEN for painting (1)
U31 – Switcher of BORDER/SCREEN for painting (2)
U32 – Output buffer of RAM
U33 – Strobe of pixels
U34C – Horizontal synchronization pulses (1)
U35 – Strobe of pixels
U36 – Generated video picture from INK, PAPER, BRIGHTNESS, FLASH
U37 – Input of keyboard (AF1) and Kempston Joystick (AF1) ports (1)
U38 – Input of keyboard (AF2) and Kempston Joystick (AF2) ports (2)
U39 – output port (AFE) keyboard/tape/audio/border
U40B – Vertical synchronization pulses (2)
U40C – Horizontal synchronization pulses (2)
U42 – Processing of data signal from tape recorder (1)
U42 – Processing of data signal from tape recorder (2)
U43 – Supply voltage regulation

Original ZX Spectrum clock frequency = 3.50000 MHz (Source: www.mk.ru.st/pdpl5/wks/sinclair48a.dir/fig/cssfag/reference/128kreference.htm)

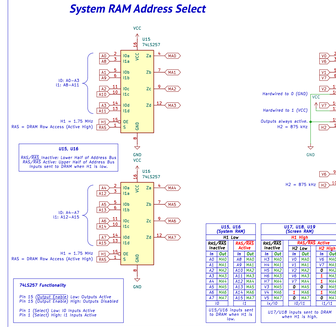
Pixel resolution (HxV): 256x192

Color grid resolution: 32x24

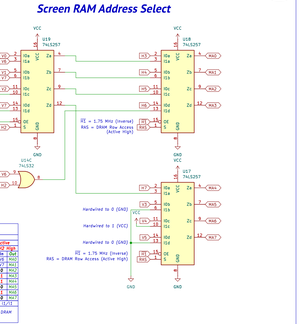
Each color grid sector contains 8x8 pixels. Aside from the two colors (out of 8 total) assigned to each sector, sectors can also be set to high or low brightness (also referred to as intensity).

As a result, the full color palette consists of 16 colors (technically 15; two of them are the same shade of black).

System RAM Address Select

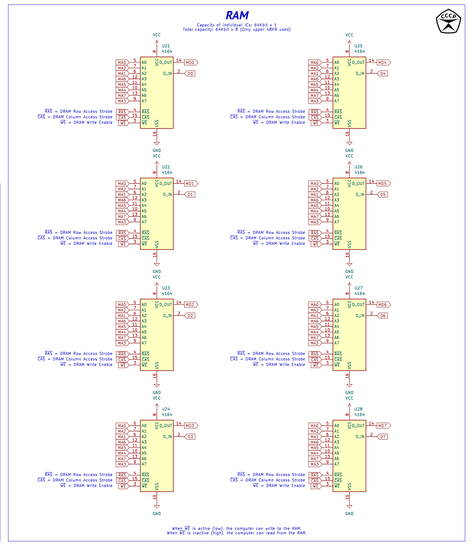


Screen RAM Address Select

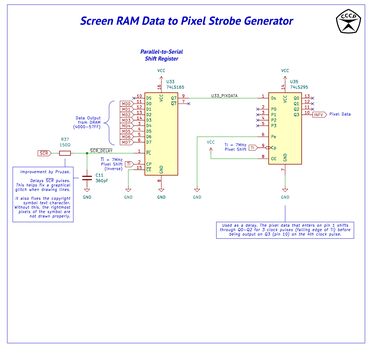


RAM

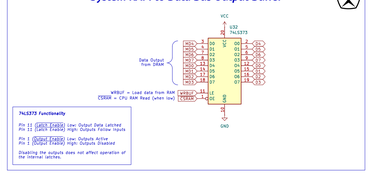
Capacity of individual Chip 8K8(8K x 8)
Total capacity: 8K8(8K x 8 (Only upper 48KB used)



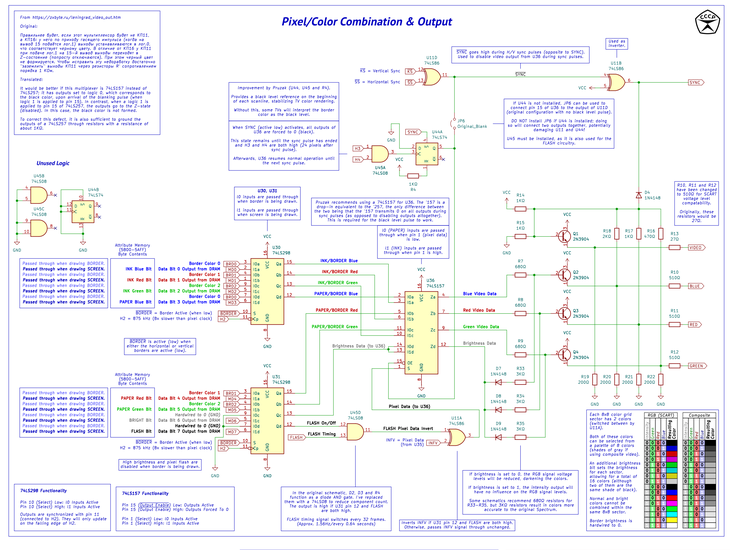
Screen RAM Data to Pixel Strobe Generator

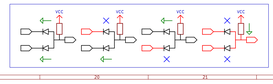


System RAM to Data Bus Output Buffer



Pixel/Color Combination & Output





DD29/DD41 in the original schematic (276k) are substituted with a 27128 (U29)
Original circuit by Sergey Zenin (ZS Research, 1988) – This schematic adapted from Z.A.N. schematic (sblive.narod.ru) – Circuit Improvements by Sergey Bagan (a.k.a. Pruzek) (zxdyte.ru) – SCART connection by Alexey (zxem.sc/a/?MkqYQL,3nX57K)

Alex Lewry
Email: zx@zxlabs.net
Site: zxlabs.net

Title: Leningrad-1 (48K ZX Spectrum Clone)

Size: A0 | Date: 2024-12-27 | Rev: 0
KiCad (5.0A, B.1) | Id: 1/1